An analytical switching model of SiC MOSFET considering the junction temperature characteristics [version 1; peer review: awaiting peer review]

Yaqiang Wang*, Qunfang Wu, Qin Wang, Lan Xiao, Junlin Zhu, Boyuan Xu, Zhifeng Sun

College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, 210067, China

First published: 16 Dec 2022, 2:19
https://doi.org/10.12688/digitaltwin.17774.1
Latest published: 16 Dec 2022, 2:19
https://doi.org/10.12688/digitaltwin.17774.1

Abstract
In order to provide convenience in the design work as the manufacturer-supplied models of silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET) are generally only applicable to specific software, an analytical switching model of SiC MOSFET considering the junction temperature characteristics based on MATLAB is proposed in this article. The junction temperature characteristics of the parameters required for the switching process, including threshold voltage, on-resistance and transfer characteristics of SiC MOSFET, threshold voltage and output characteristics of body diode, which are extracted from the datasheet of the SiC MOSFET provided by the manufacturer. Then a model for the transient process of the test circuit, including the non-linear capacitance, the parasitic resistance and parasitic inductance from package and the printed circuit board is created. After that, each sub-stage of the switching process is analyzed in detail, then the analytical model is solved numerically using MATLAB. Finally, the SiC MOSFET C3M0075120K manufactured by Wolfspeed is selected as the case study to verify the built model, and the accuracy is validated by comparing with the LTspice simulation and experiment results. As a result, the proposed model can be applied, especially in designs involving junction temperatures.

Keywords
analytical model, junction temperature, silicon carbide (SiC) MOSFET, body diode, switching transient process.
Corresponding author: Qunfang Wu (wuqunfang@nuaa.edu.cn)

**Author roles:** Wang Y: Data Curation, Formal Analysis, Investigation, Methodology, Software, Validation, Writing – Original Draft Preparation, Writing – Review & Editing; Wu Q: Conceptualization, Project Administration, Resources, Supervision; Wang Q: Resources, Supervision; Xiao L: Funding Acquisition, Resources, Supervision; Zhu J: Methodology, Writing – Review & Editing; Xu B: Methodology, Writing – Review & Editing; Sun Z: Methodology, Writing – Review & Editing

**Competing interests:** No competing interests were disclosed.

**Grant information:** This research work has been supported in part by grants from the Delta Power Electronics Science and Education Development Program of Delta Group, in part by grants from the Natural Science Youth Foundation of Jiangsu Province (BK20210305), in part by National Natural Science Foundation (52177049), in part by NUAA prospectively layout scientific research project (1003-ILA220531A22) and in part by the Key Project of Experimental Technology Research and Development of Nanjing University of Aeronautics and Astronautics in 2021.

The funders had no role in study design, data collection and analysis, decision to publish, or preparation of the manuscript.

**Copyright:** © 2022 Wang Y et al. This is an open access article distributed under the terms of the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

**How to cite this article:** Wang Y, Wu Q, Wang Q et al. An analytical switching model of SiC MOSFET considering the junction temperature characteristics [version 1; peer review: awaiting peer review] Digital Twin 2022, 2:19
https://doi.org/10.12688/digitaltwin.17774.1

**First published:** 16 Dec 2022, 2:19 https://doi.org/10.12688/digitaltwin.17774.1

This article is included in the Digital Twin International Conference 2022 Collection collection.
Introduction
In recent years, with the rapid development of manufacturing technology and process level, the production cost of silicon carbide (SiC) metal oxide semiconductor field effect transistor (MOSFET) has been directly reduced, making the application of SiC MOSFET more and more varied. Therefore, the accuracy of the SiC MOSFET model is important in the converter design, power loss estimation and so on. Junction temperature is an important parameter that should not be ignored in the filed application, life prediction and reliability analysis. Although a lot of research has been done on the temperature characteristics of SiC MOSFET, there are varying study results both in industry and academic fields.

The SiC MOSFET in papers\(^4\)\(^-\)\(^6\) is set up using the traditional silicon (Si) MOSFET modeling method, supplemented and optimized successively, by describing several discrete temperature points from the beginning, and then adding the low temperature characteristic of the SiC MOSFET threshold voltage. However, this kind of model does not take into account the temperature characteristics of the core part of the device, and only compensates for the external one, so the temperature-related characteristics of a SiC MOSFET cannot be guaranteed. The drain current and body diode current of a SiC MOSFET in the model proposed in paper\(^8\)\(^-\)\(^9\) are fitted with a hyperbolic tangent function according to the output and transfer characteristic curves. Although the core part of the device is modeled, it is impossible to accurately describe the characteristics of SiC MOSFET only by a single function, especially in the transient process, which differs from the experiment, and it is impossible to reflect the changes of temperature-sensitive parameters. A wide temperature range model for SiC MOSFETs is presented in paper\(^2\), but the physical coefficients involved in the model are difficult to obtain, and the model only considers the static characteristics of a SiC MOSFET. The analysis in 8 is very detailed, however, the model used only considers the temperature characteristics of threshold voltage and on-resistance, and does not accurately describe the relationship between the corresponding parameters and temperature using only first-order linear and exponential fitting, respectively. The model proposed in 9 considers that threshold voltage, saturated drain voltage and saturated drain current which are affected by junction temperature, and the description of characteristics in the switching process is insufficient. The work in paper 10 presents a step-by-step modeling method for a SiC MOSFET half-bridge power module, which considers the temperature characteristics of the drain current of a SiC MOSFET, but it ignores the effect of junction temperature on the body diode, and still has some space for the optimization.

In this paper, an analytical switching model of SiC MOSFET considering the junction temperature characteristics is presented based on MATLAB (RRID:SCR_001622)\(^(an\ open-source\ alternative\ that\ may\ perform\ similar\ tasks\ GNU\ Octave)\). The drain current, body diode and parasitic capacitance are accurately modeled according to the manufacturer datasheet. The junction temperature dependence of threshold voltage, on-resistance and transfer characteristics of the SiC MOSFET, threshold voltage and output characteristics of body diode are considered. The model is verified by comparing with LTspice (17.0.35.0) simulation and experimental data. This modeling method can be easily applied to other SiC MOSFETs to facilitate device analysis and system design. This paper chooses C3M0075120K SiC MOSFET (1200V/32A) as the case study.

Model parameters
The model parameters of a double pulse test (DPT) circuit using two of the same SiC MOSFETs in series are described in this section. The main parasitic parameters are taken into account in the DPT circuit, as shown in Figure 1.

The model parameters mainly include resistance, parasitic inductance, parasitic capacitance and temperature-sensitive electrical parameters (TSEPs).

Resistance and parasitic inductance
The resistances in considered in this model include the gate resistance ($R_g$), the on-resistance of the SiC MOSFET ($R_{d(on)}$), and the parasitic resistance in the power circuit ($R_{p1}$, $R_{p2}$), as shown in Figure 1. The gate resistance ($R_g$) is the sum of the drive resistance, drive circuit parasitic resistance and the internal gate resistance. On-resistance ($R_{d(on)}$), the equivalent resistance of the SiC MOSFET in the amplifier region, varies with junction temperature, which is detailed in the “Temperature-sensitive electrical parameters” section. Parasitic resistances $R_{p1}$ and $R_{p2}$ distribute part of the voltage in the circuit and determine the attenuation degree of oscillation waveform.

Figure 1. Double pulse test (DPT) circuit.
The parasitic inductances of the model include power circuit parasitic inductance \(L_{gs}, L_{gs}, L_{gs}, L_{gs}, L_{gs}, L_{gs} \) which are combinations of SiC MOSFET pins parasitic inductance \(L_{gs}, L_{gs}, L_{gs}, L_{gs} \) and part of the parasitic inductance values in the loop, as shown in Figure 1.

Parasitic capacitance

Similar to the method in paper 11, the \(C_{x}, C_{x}, C_{x} \) curves in the datasheet are fitted according to the following formula:

\[
C_{xx}(v) = C_{xx} - C_{xx} + C_{xx}, \quad x = r, t, o
\]

where \(C_{xx} \) and \(C_{xx} \) are the maximum and minimum capacitance of target capacitors, respectively, and \(V_{th} \) and \(r \) are the parameters to be fitted.

Temperature-sensitive electrical parameters

Temperature-sensitive electrical parameters (TSEPs) include threshold voltage \(V_{th}, \) on-resistance \(R_{ds(on)} \), transfer characteristics of the SiC MOSFET, threshold voltage of body diode \(V_{th,bd} \), and output characteristic of body diode.

1) Threshold voltage \(V_{th} \): Similar to the papers 9, 12, the temperature curve of threshold voltage in the datasheet is fitted in the second order as follows:

\[
V_{th} = k_1 \cdot T^2 + k_2 \cdot T + k_3
\]

2) On-resistance \(R_{ds(on)} \): According to the on-resistance curve in the datasheet, it is known that the value is affected by the drain current \(I_d \) on the gate-source voltage \(V_{gs} \) and the junction temperature \(T_J \). In order to simplify the model, only the latter two are considered. Referring to the method in 6, the second-order temperature fitting of the on-resistance is performed, and then the second-order fitting of the fitted coefficient to the gate-source voltage \(V_{gs} \) is performed, as follows:

\[
R_{ds(on)} = k_4 \cdot T^2 + k_5 \cdot T + k_6
\]

\[
k_4 = m_1 \cdot V_{gs}^2 + m_2 \cdot V_{gs} + m_3
\]

\[
k_5 = m_4 \cdot V_{gs}^2 + m_5 \cdot V_{gs} + m_6
\]

\[
k_6 = m_7 \cdot V_{gs}^2 + m_8 \cdot V_{gs} + m_9
\]

3) Transfer characteristics of a SiC MOSFET: By comparing several common fitting forms in paper 11, the following fitting form is better:

\[
i_{ch} = a \cdot (V_{gs} - V_{th})^b
\]

Therefore, on the basis of (7), considering the effect of junction temperature, a second-order temperature fitting is made for its coefficients, as shown below:

\[
a = k_7 \cdot T^2 + k_8 \cdot T + k_9
\]

4) Threshold voltage of body diode \(V_{th,bd} \): Similar to conventional diodes, the body diode of SiC MOSFET has an on-voltage driven by a fixed negative gate-source voltage, which is also affected by the junction temperature. Similar to threshold voltage \(V_{ds} \), the threshold voltage of the body diode \(V_{th,bd} \) also is fitted in the second order as follows:

\[
V_{th,bd} = k_{13} \cdot T^2 + k_{14} \cdot T + k_{15}
\]

5) Output characteristic of body diode: For DPT circuits, the body diode of the SiC MOSFET has a great influence on the switching process, so it is necessary to take its output characteristics into account. In this paper, the output characteristics of body diode is fitted as follows, referring to the fitting method of transfer characteristics of a SiC MOSFET:

\[
i_{bd} = c \cdot \left(\frac{V_{bd}}{V_{th,bd}}\right)^d
\]

\[
c = k_{16} \cdot T^2 + k_{17} \cdot T + k_{18}
\]

\[
d = k_{19} \cdot T^2 + k_{20} \cdot T + k_{21}
\]

Proposed model

The modeling method used here is similar to the SiC MOSFET hard switch analysis model in the paper 13,14,15. The difference is that the TSEPs are added, and five state variables are introduced: channel current \(I_{ch} \), gate-source voltage \(V_{gs} \), drain current \(I_d \), drain-source voltage \(V_{ds} \), body diode voltage \(V_{th,bd} \). These five state variables are solved according to the state space equation.

During the switching process, \(S_2 \) goes through three different stages: cutoff zone, amplification zone and saturation zone, and their output characteristics are different in different stages. Using the classical model in 9,10 as reference, channel currents in these three regions are described separately:

**Cutoff zone** \((V_{gs} < V_{th})\):

\[i_{ch} = 0\]

**Saturation zone** \((V_{gs} > V_{th}, V_{ds} > V_{gs} - V_{th})\):

\[i_{ch} = a \cdot (V_{gs} - V_{th})^b\]

**Amplification zone** \((V_{gs} > V_{ds}, V_{ds} < V_{gs} - V_{th})\):

\[i_{ch} = V_{ds} / R_{ds(on)}\]

This paper mainly studies the switching on and off process of SiC MOSFET in the test circuit. There are several sub-stages during the switching transient process, each of which has different characteristics. Figure 2 shows the equivalent circuit of different sub-stage.
Turn-on process
There are five sub-stages during the turn-on process.

1) Sub-stage 1\([t_0-t_1]\)
At \(t_0\), the gate-driver voltage \(V_{GH}\) is high, the gate current \(i_g\) starts to charge the input capacitance \(C_{iss}\), and the gate-source voltage \(V_{gs}\) begins to increase from the negative voltage. During this process, the SiC MOSFET channel has not been formed and the drain has no current. From Figure 2(a), the expressions (14), (17–20), (23) can be obtained.

This sub-stage ends when the gate-source voltage \(V_{gs}\) reaches the threshold voltage \(V_{th}\).

2) Sub-stage 2\([t_1-t_2]\)
At this stage, the SiC MOSFET channel has been formed. The drain current \(i_d\) starts to increase from 0 and the drain-source voltage \(V_{ds}\) decreases. Meanwhile, the current of body diode decreases gradually. From Figure 2(b), the expressions (15), (17–20), (23) can be obtained.

When \(V_{bd} < V_{th-bd}\), the body diode is turned off, and the sub-stage ends.

3) Sub-stage 3\([t_2-t_3]\)
At this stage, the drain current \(i_d\) continues to increase and the drain-source voltage \(V_{ds}\) continues to decrease. When the drain...
current $i_j$ reaches the inductance current $I_L$, the drain current continues to increase due to the reverse recovery characteristic of the body diode. From Figure 2(c), the expressions (15), (17–21) can be obtained.

When $dt_j / dt = 0$, the drain current $i_j$ reaches the peak current $I_\text{peak}$ and the sub-stage ends.

4) Sub-stage 4[$t_r$–$t_s$]

At this stage, the drain current $i_j$ begins to decrease, the drain-source voltage $V_{ds}$ continues to decrease, and the reverse recovery current of the body diode decreases exponentially. The SiC MOSFET stays in the saturated region, and its channel current $i_s$ varies according to expression (15). From Figure 2(c), the expressions (15), (17–20), (22) can be obtained.

When $V_{ds} < V_{gr} - V_{ao}$, SiC MOSFET transitions from saturation zone to amplification zone, and this sub-stage ends.

5) Sub-stage 5[$t_s$–$t_e$]

At this stage, the SiC MOSFET enters into the amplification zone, the transfer characteristic curve is not applicable, and the channel current $i_s$ is affected by $R_{ds(on)}$ and $V_{gr}$. The drain current $i_d$ enters into the oscillating stage. From Figure 2(d), expressions (16–20), (22) can be obtained.

This stage continues until the SiC MOSFET is turned off.

Turn-off process

Slightly different from the turn-on process, the turn-off process can be divided into four sub-stages,

1) Sub-stage 1[$t_r$–$t_s$]

At $t_r$, the gate-driver voltage $V_{GHi}$ is negative, the gate current $i_g$ starts to discharge the input capacitance $C_{ss}$, and the gate-source voltage $V_{gs}$ begins to decrease gradually from the positive voltage. During this process, the SiC MOSFET remains in the amplified zone and the channel current varies according to (16). From Figure 2(c), the expressions (16–21) can be obtained.

When $V_{gh} > V_{gs} - V_{ao}$, the SiC MOSFET transitions from amplification zone to saturation zone, and this sub-stage ends.

2) Sub-stage 2[$t_s$–$t_e$]

At this stage, the gate-source voltage $V_{gs}$ continues to decrease, the SiC MOSFET has entered into the saturation zone, and the channel current $i_s$ varies according to the expression (15). From Figure 2(c), the expressions (15), (17–21) can be obtained.

When $V_{gs} < V_{ao}$, SiC MOSFET turns off, channel current $i_s$ is reduced to 0, the sub-stage ends.

3) Sub-stage 3[$t_e$–$t_f$]

At this stage, the SiC MOSFET channel remains closed, the channel current $i_s$ remains 0, the drain current $i_j$ continues to decrease, the output capacitance of the body diode continues to discharge, and its voltage continues to decrease. From Figure 2(b), the expressions (14), (17–21) can be obtained.

When $-V_{bd} > V_{th,ao}$, the body diode starts to conduct and the sub-stage ends.

4) Sub-stage 4[$t_f$–$t_e$]

At this stage, the body diode remains conductive, its output current varies according to (11), the SiC MOSFET is cut off, the drain current $i_d$ and the drain-source voltage $V_{ds}$ vary according to (17–20), (23) can be obtained.

This stage continues until the SiC MOSFET is turned on by a positive $V_{GHi}$

\[ i_d = i_{ch} + C_{oss} \frac{dV_{ds}}{dt} - C_{gd} \frac{dV_{gs}}{dt} \] (17)

\[ V_{in} = V_{ds} + L_{loop} \frac{di_d}{dt} + (R_{p1} + R_{p2})i_d + V_{bd} \] (18)

where, $L_{loop} = L_{p1} + L_{ps} + L_{d1} + L_{s} + L_{in} + L_{s2}$

\[ V_{GHi} = R_{g}i_d + (L_{g2} + L_{ks2}) \frac{di_d}{dt} + V_{gs} \] (19)

\[ i_g = C_{oss} \frac{dV_{gs}}{dt} - C_{gd} \frac{dV_{ds}}{dt} \] (20)

\[ \frac{dV_{bd}}{dt} = \frac{1}{C_{oss}} (i_d - I_{in}) \] (21)

\[ \frac{dV_{bd}}{dt} = \frac{1}{C_{oss}} (i_d - I_{in}) + R_s \frac{di_d}{dt} \] (22)

\[ \frac{dV_{bd}}{dt} = \frac{1}{C_{oss}} \left[ i_d - I_{in} + c(-V_{bd} - V_{th,bd}) \right] \] (23)

Verification of the proposed model

Experimental setup

The DPT setup is designed for experimental verification, as shown in Figure 3. The SiC MOSFET C3M0075120K from Wolfspeed was used. The control signal was generated by a Texas Instruments TMS320F28335 digital signal processor (DSP) board. The hot plate provides test environment at different temperatures, ranging from 25°C to 150°C. The negative gate-driver voltage is -4V so that exceptions such as crosstalk are unlikely to occur. The experimental parameters, including the parasitic resistances and parasitic inductances, are shown in Table 1.

Junction temperature fitting

The expression (1) is used to fit the nonlinear capacitance of C3M0075120K. The extracted fitting coefficients are given in Table 2 and the fitting curves are shown in Figure 4. The results are highly consistent with the data.
Meanwhile, the TSEPs are fitted according to the expressions (2)~ (13), and the fitting coefficients are shown in Table 3. Figure 5–Figure 9 show the fitting results respectively. The curves are fitted well.
Figure 5. Fitting results of threshold voltage.

Figure 6. Fitting results of transfer characteristic.

Figure 7. Fitting results of on-resistance.
Figure 8. Fitting results of output characteristic of body diode.

Figure 9. Turn-on process at $T_j = 25\, ^\circ C$.

Verification

The model is implemented in MATLAB and compared with LTspice simulation and experiment at $T_j = 25\, ^\circ C$ as shown in Figure 9–Figure 10. The consistency of waveforms is high.

Meanwhiles, the validation is carried out in a wide range of junction temperatures from 25°C to 150°C. Figure 11–Figure 12 are the switching transient waveforms obtained by the proposed temperature model in MATLAB at different junction temperatures. Figure 13–Figure 14 are the switching transient waveforms simulated by LTspice at different junction temperatures. Figure 15–Figure 16 are the switching transient waveforms obtained from the experiments at different junction temperatures. The analysis shows that the transient waveform of the switching process has the same trend under different junction temperatures, and the degree of coincidence is high, which verifies the correctness of the proposed temperature model.
Figure 10. Turn-off process at $T_j = 25^\circ$C.

Figure 11. Turn-on process of the proposed model at different $T_j$.

Figure 12. Turn-off process of the proposed model at different $T_j$. 

Digital Twin 2022, 2:19 Last updated: 16 DEC 2022
Figure 13. Turn-on process in LTspice simulation at different $T_j$.

Figure 14. Turn-off process in LTspice simulation at different $T_j$.

Figure 15. Turn-on process in experiment at different $T_j$. 
Figure 16. Turn-off process in experiment at different $T_j$.

Conclusions
In order to study the effect of junction temperature on the switching process of SiC MOSFET, a precise model of a SiC MOSFET considering the junction temperature effect is presented. The model considers all TSEPs and parasitic elements in the circuit and has a high goodness of fit with LTspice simulation and experiments. Furthermore, the method can be applied in any SiC MOSFET which may provide a convenient way for power electronics engineer. At the same time, it is undeniable that there are still some differences between the model and the experiments, because the parasitic parameters cannot be completely consistent with the actual situation, and the measurement device has errors in the ns-level measurement, and so on. The model still has room for optimization.

Data availability
Underlying data
Zenodo: an analytical switching model of SiC MOSFET. https://doi.org/10.5281/zenodo.7238381

This project contains the following underlying data
- GateThresholdVoltage1.xlsx (Data of Threshold voltage)
- Rds_on1.xlsx (Data of on-resistance)
- Turn off data in LTspice.xlsx
- Turn off data in experiment.xlsx
- Turn on data in LTspice.xlsx
- Turn on data in experiment.xlsx
- Body diode1.xlsx (Data of body diode)
- capacitance3.xlsx (Data of capacitances)
- trans1.xlsx (Data of transfer characteristics)

Data are available under the terms of the Creative Commons Attribution 4.0 International license (CC-BY 4.0).

Software availability
Archived source code at time of publication: https://doi.org/10.5281/zenodo.7269179

License: GNU v1.0

References
7. Shimozato K, Bian S, Sato T: A Compact Device Model for SiC MOSFETs Valid


